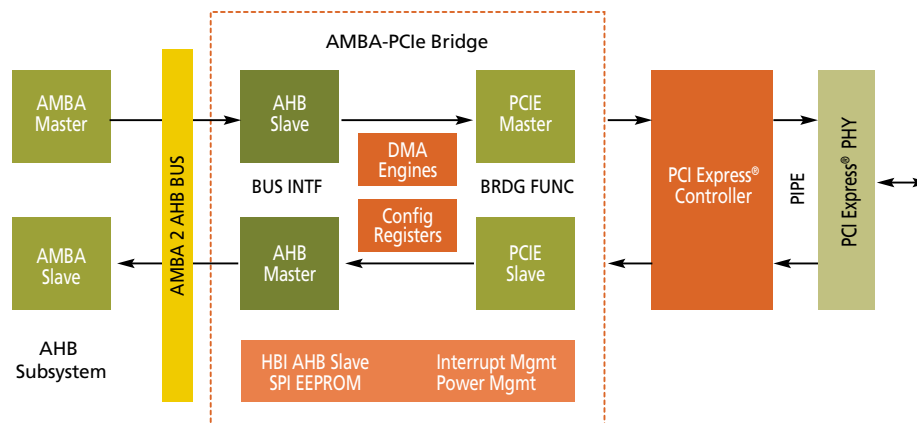


PCI Express® AMBA™ 2 AHB® Bridge

LOW SILICON FOOTPRINT, LOW LATENCY AND MAXIMUM THROUGHPUT CORES



FEATURE HIGHLIGHTS

- Low Latency and High Throughput Architecture
- Supports PCI Express® Base Specification 1.1 and 2.0
- Choice of either Root Mode or Endpoint Mode for PCI Express® at Power-up
- Supports MSI or Legacy Interrupt for PCI Express
- Supports system interrupt for ARM or Internal processor
- Supports EEPROM controller to load boot data through SPI interface
- Support Mailbox between PCI Express® and AMBA 2 AHB Bus
- Supports Error Handling of both PCIe and AHB Protocols

POWER MANAGEMENT

- Supports all required and optional PCI Express® power management states: L0, L0s, L1, L2 & L3
- ClkReq mechanism for low power mode in mobile form factors
- Supports Beacon and Wake-Up mechanism on PCIe Link

HIGH THROUGHPUT

- Supports 1st Party DMA with ability to accept DMA Memory WR/RD commands from PCIe and AMBA Master.
- Multiple descriptors per DMA channel
- Handles out-of-order read-completions from PCIe targets
- Supports wrap cycles on the AMBA AHB bus
- Local CPU Off-load Support through Concurrent DMA Write and Read

FLEXIBLE ADDRESSING/DATAWIDTH

- Supports both 32b/64b addressing from PCIe to AHB bus
- Configurable AMBA Databus - Master and Slave independently configurable to either 32-bit or 64-bit
- User selectable 5 variable windows from AMBA to PCIe address translations
- User selectable 4 variable windows from PCIe to AMBA address translations
- Up to 4 Base Address Registers (BARs) available in root mode address translation

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INTERRUPT/MAILBOX

- Interrupt generation from local CPU to external CPU
- Interrupt generation from external CPU to internal CPU
- Mailbox interrupt registers from internal CPU to external CPU
- Mailbox interrupt registers from external CPU to internal CPU

BRIDGE REGISTERS

- Dedicated Bridge internal registers in PCIe clock domain for software accessibility during internal power save
- Bridge internal registers accessible from both PCIe and AMBA bus

ARCHITECTURE

- Architected by industry veterans with many years of SoC expertise
- Highly Scalable & Pipelined Architecture
- Designed for low power application
- Easily configurable Plug-and-Play User Logic Interface
- Optimized architecture with multiple datapath widths
- Design for Testability (DFT) and Design for Debugability (DFD) features
- Technology independent design for ASIC/FPGA
- Low Silicon Footprint - Suitable for Multiple Instances of the Core in Single ASIC/FPGA

PARAMETERIZED CORE

- Highly Parameterized RTL for easy configurability depending on your custom requirements
- Supports both Cut-Through and Store-and-Forward schemes for forwarding transmitted packets
- User configurable Virtual Channels and Traffic Class mapping
- Selectable ECRC and Advanced Error Reporting Support

PLUG-N-PLAY TYPE APPLICATION INTERFACE

- Easy-to-Integrate Interface with User Logic
- Streamlined User Interface with reasonable number of interface signals
- Controllability for critical device parameters

DELIVERABLES

- Synthesizable Verilog RTL
- Sample Testbench for Simulation
- Sample Synthesis Scripts
- Sample Static Timing Analysis
- User Manual and Application Note

LEARN MORE:

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