

DDR I/II Controller Core

Product Overview

ASIC Architect's DDR I/II Controller Core is an integral part of the product portfolio aimed at providing a complete end-to-end solution in the High Speed Interface Controller domain. The DDR I/II Controller Core has been architected, designed and verified by ASIC/SoC industry veterans. The add-on solution cores that come with the DDR Controller accelerate the chip-level integration by connecting multiple clients to the DDR Controller.

Product Features

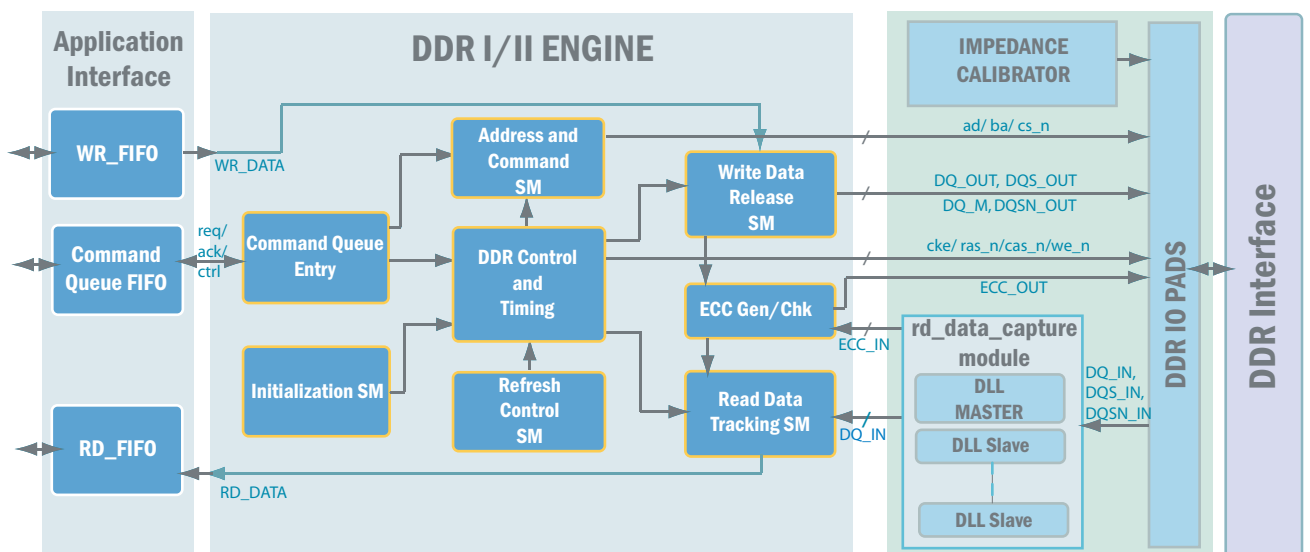
- Powerful Application Interface
- Supports both DDR I and DDR II JEDEC Standards
- Addressing capability upto 4GB DDR2 devices
- Programmable Features:
 - Memory timing parameters - T_{ras} , T_{rdl} , T_{wr} , T_{ccd} , T_{rfc} , T_{mrd} , T_{rp} , T_{crd}
- Intelligent Bank Management
- Supports buffered and unbuffered DIMMs
- Supports On-die termination (ODT), and Off-Chip Driver impedance adjustment
- Configurable Features:
 - Address Mapping between application bus and row/column/bank addresses
 - Choice of 16/32/64-bit DDR bus-width
 - Size of Command Queue
- Supports addition CAS latency feature to maximize command bus utilization
- Supports Back-to-Back WR & RD with minimum time intervals

Product Features

- High data rate upto 100% memory throughput
- Byte-wide optional ECC Support
- Auto initialization of DDR Memories
- Byte-Wide Data Mask Support
- Self-refresh and power down control
- Fully ATPG Testable - Multiple Clock Domains
- Supports upto 800MHz in DDR II Mode
- Supports industry standard memory vendors
- Low Gatecount
- Low Latency
- Verified with leading memory and IO vendors
- Supports Multiple Application Clients

ASIC Deliverables

- Synthesizable Verilog RTL
- Testbench and Models for Simulation
- Complete User Integration Manual
- Sample Synthesis and Static Timing Analysis Scripts
- Support from Core Integration through Silicon Bring-Up



Low Silicon Footprint, Low Latency and Maximum Throughput Cores